IEEE ITALY SECTION
IA/PEL C&S Italy Joint CHAPTER
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ROMA TRE
UNIVERSITÀ DEGLI STUDI

ECPE Competence Centre

Roma Tre Summer Course on

Power Electronics and Applications

Organizer and Host Institution Roma Tre University – Department of Engineering, Power Electronics and Electric Drives Laboratory, luca.solero@uniroma3.it

Technical Sponsorship ECPE – European Center for Power Electronics

In cooperation with

Chairman Fabio Crescimbini - *Roma Tre University*

Lecturers
Stefano Bifaretti - *University of Roma Tor Vergata*
Valeriano Cardi – *Semikron*
Jesus Doval-Gandoy – *University of Vigo*
Petar Grbovic (IEEE Distinguished Lecturer) – *University of Innsbruck*
Marco Lega - *ABB*
Alessandro Lidozzi, Luca Bigarelli - *Roma Tre University*
Leo Lorenz – *ECPE*
Myriam Desranleau, Yoann Mougenot– *OPAL RT Technologies*
Vladimir Scarpa – *STMicroelectronics*

The course is scheduled in 2 weeks, 5 days a week, 30 hours lessons, 3 ECTS each week. Lecturers will be held during the 1st week, laboratory activities will take place during the 2nd week of the course. Each course week can be attended independently and as a single short course. The course is primarily intended for PhD and Master students; however, it is also open to staff of companies interested in the topic.

No fees for attending people.

Registration Register before June 21st, 2019.
Please email a copy of the completed registration form to luca.solero@uniroma3.it

Venue Roma Tre University, Department of Engineering
Via della Vasca Navale, 79 – 00146 Roma, Italy
Mechanical and Industrial Engineering Division, 2nd floor
Conference Room n. dir.01, Ph. +39 06 5733 3277

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OPAL-RT TECHNOLOGIES
i-PEL Innsbruck Power Electronics Lab.
ABB
APET Applied Power Electronics Technology Research Group Universidad de Vigo
Università di Roma Tor Vergata

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2019 Roma Tre Summer Course on Power Electronics and Applications	
Registration Form (email to luca.solero@uniroma3.it) Week 1, July 1-5 ☐ Week 2, July 8-12 ☐	
Attendee:	
	Title, Given Name, Name
	Company, Department
	Full Address
	Phone, Fax
	Email
	Date, Signature

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Week 1 (3 ECTS) - Power Electronics in E-Mobility Applications

Monday, July 1st

10.15-10.30	Welcome, Introduction	F. Crescimbini
10.30-12.45	DC Chargers for Electrical Vehicles today and tomorrow: concepts, topologies and semiconductor devices - Part I	V. Scarpa
14.00-15.45	DC Chargers for Electrical Vehicles today and tomorrow: concepts, topologies and semiconductor devices - Part II	V. Scarpa
16.00-17.45	Design of Power Modules	V. Cardi

Tuesday, July 2nd

09.15-11.00 11.15-13.00	OPAL-RT solutions for power electronics real-time simulation on NI chassis	M. Desranleau Y. Mougenot
13.45-18.00	Tour at Semikron Italy Factory	V. Cardi

Wednesday, July 3rd

09.15-11.00	High Power Fast DC Charging System for EVs - Part I	M. Lega
11.15-13.00	High Power Fast DC Charging System for EVs - Part II	M. Lega
14.00-15.45	AC Current Control of Grid-Tied Converters – Part I	J. Doval-Gandoy
16.00-17.45	Development Trend of Si and WB Devices – What is required by the Application, Part I	L. Lorenz

Thursday, July 4th

09.15-11.00	AC Current Control of Grid-Tied Converters – Part II	J. Doval-Gandoy
11.15-13.00	Development Trend of Si and WB Devices – What is required by the Application, Part II	L. Lorenz
14.00-15.45	Power Converters and Chargers for e-mobility Applications	P. Grbovic
16.00-17.45	High Performances Phase and Frequency Estimation Techniques for Grid-Connected Converters: from theory to practical implementation	S. Bifaretti A. Lidozzi

Friday, July 5th

09.15-11.00	Partial Power Processing Converters- A Way to go Beyond The Limits	P. Grbovic
11.15-12.45	Multiple Choice Survey	L. Solero

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Week 2 (3 ECTS) - Practice on Power Electronics (Hands-on class)

Instructors: A. Lidozzi, L. Bigarelli, S. Bifaretti

Monday July 8th 11.30-13.00 and 14.00-17.45
Tuesday July 9th 09.15-12.45 and 14.00-17.45
Wednesday July 10th 09.15-12.45 and 14.00-17.45
Thursday July 11th 09.15-12.45 and 14.00-17.45
Friday July 12th 09.15-13.30

Introduction

Nowadays, even a common power converter can exhibit an increased number of active devices and higher switching frequency than ever to satisfy a higher control performance demand. This results in an increased complexity related to the control board, where usually a combined C (or P, DSP) and FPGA are both installed. Those two 'actors' require a completely different programming approach and development tools from those employed by traditional boards.
Accordingly, control algorithm development is considered a 'time consuming' task within a research or industrial project. IDE (Integrated Development Environment), provided by the control platforms manufacturers or third parties, are constantly moving from the classical, old, text-based approach to a new, fast and simple to learn graphical programming method. Moreover, a high level of abstraction is usually requested in order to accelerate the learning time even on non-specialist workers; however, a full control on the hardware is still mandatory.
This hands-on week will cover the methodologies to switch to the newly graphical programming development environments, starting from a review and going into the most promising solutions.
Code splitting between targets, best practices, and code efficiency will be part of the tutorial.
The usage of FPGA has some inherent drawbacks such as the long compiling time: FPGA co-simulation and hardware-in-the-loop techniques will be also covered to help the designer workflow.

Outline

Theory and practice with the National Instruments sbRIO-9651 and Linux real-time OS. Insight view and develop of specific Power Electronics and Drives applications using LabVIEW integrated development environment.

- LabVIEW basic concepts, front panel and block diagram, debugging, programming guidelines. Application development. Graphical programming of the Real-Time and FPGA targets. Communication between targets. Code efficiency and best practices.
- Development of the FPGA main scheduler and synchronization with the on board μProcessor, PWM modulator with configurable dead-time.
- Floating-point math operations on FPGA target. (*a must have!*)
- Development of high performance control algorithms such as repetitive control, resonant controllers, Model Predictive Control and combined control structures. Code splitting between targets. Insight view of PWM modulators for multilevel power converter topologies.
- LabVIEW FPGA/ NI-Multisim co-simulation, a very powerful tool to test the developed FPGA code.
- Closed loop tests with the Hardware-in-the-loop simulator.
- Code verification on a real power converter platform.
- Discussion on the lab sessions.

Control board info: www.ped-board.com

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